Dual Boost High Performances Power Factor Correction (PFC) control strategy implemented on a low cost FPGA device, using a custom *sfloat24* developed math library

F. Parillo
Department of Electrical Engineering and Information University of Cassino, Via G. Di Biasio 43, I-03043 Cassino (FR) - ITALY
f.parillo@unicas.it

Abstract ─ In this paper are described a PI controller and an Active Filtering control strategy, applied to a Dual Boost Power Factor Correction (PFC) implementation, on a low cost FPGA device, using a custom developed *sfloat24* math library.
The implemented control strategy consists in an optimized power sharing where the active filtering approach is used to increase the current quality and at the same time to reduce the switching losses.
The simulation results show that the *sfloat24* floating point, IEEE 754 compliant, digital PI controller and the active filtering approach outperform by high-speed response, better precision, minor error and high dynamic range.
Both the simulation and experimental results show that the adopted control strategy for PFC achieves near unity power factor and a not negligible switching losses reduction.

Index Terms — FPGA, *sfloat24* math library, Power Factor Correction (PFC).

I. INTRODUCTION

The Proportional–Integral–Derivative (PID) controller is one of the most common types of feedback controllers that are used in dynamic systems. This controller has been widely used in many different areas, such as aerospace, process control, manufacturing, robotics, automation, and transportation systems. Implementation of PID controllers has gone through several stages of evolution, from early mechanical and pneumatic designs to microprocessor-based systems. Recently, Field-Programmable Gate Arrays (FPGAs) have become an alternative solution for the realization of digital control systems, which were previously dominated by general-purpose microprocessor systems [1].
The FPGA is a programmable digital logic device by software. Thus, it can execute any logical function such as numeric processors, digital interface, controllers and decoders only in a single IC. The FPGA architecture contains programmable logic components called Configurable Logic Blocks (CLB), and a hierarchy of reconfigurable interconnects that allow the blocks to be wired together. The CLB can be configured to make complex combinational functions, or only simple logic gates like AND and XOR.
In most FPGA, the CLB also include memory elements, which can be simple flip-flops or more complete blocks of memory. FPGAs are programmed using a logic circuit diagram or a source code in Hardware Description Language (HDL) [2].

The fixed-point arithmetic allows the computations to be performed with a high precision according to the bit width representation. However, many applications, for example a PI controller implementation, require to work not only with a high precision, but also with a suitable format in order to represent large and small real numbers. Therefore, the floating-point arithmetic is a feasible solution for high performance computer systems, providing a dynamic range for representing real numbers and capabilities to retain its resolution and accuracy.
In the hardware design of floating-point units it is very important to address two main aspects: (a) the choice of a suitable bit-width in a such way that dynamic range is large enough to guarantee that saturation will not occur for a general-purpose application and (b) the trade-off between the level of precision of the operators against their implementation cost in logic area [3].

Nowadays, the switching power converters are very important circuits in many industrial applications and in several household appliances.
Compared with a traditional linear power converter, a switching power converter has many features like: fast dynamic response; simple control; high efficiency wide input voltage range; high power density and a reduced size and weight. The Power Factor Correction (PFC) converters are necessary for a lot electronic equipment. This is due to the greater focus on energy efficiency and the implementation of regulations such as international standard IEC61000-3-2 that specifies the maximum allowable harmonic currents. A number of power factor correction circuits have been developed recently, which has been used as a popular solution to suppress current harmonics [4].

II. IMPLEMENTED CONTROL STRATEGY

The full implemented control strategy (PI controller and Active Filtering approach) on a Dual Boost PFC converter is shown in the following Fig.:

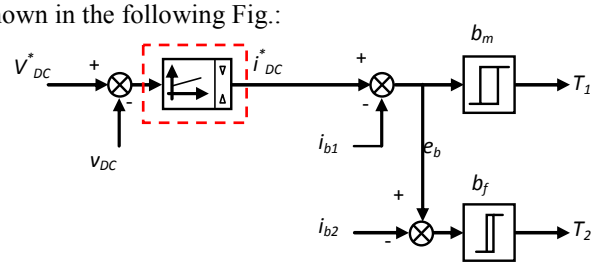


Fig. 1. Scheme of the implemented control strategy

In this case, the control strategy is based on a dual boost circuit where the first one (T_{b1} switch and L_{b1} inductor) is used as main PFC circuit and where the second one (T_{b2} switch and L_{b2} inductor) is used to perform an active filtering. The purpose of the active filtering performed by the second boost circuit is to increase the quality of the line current and at the same time to reduce the PFC total switching losses. The implemented power converter is shown in the following Fig.

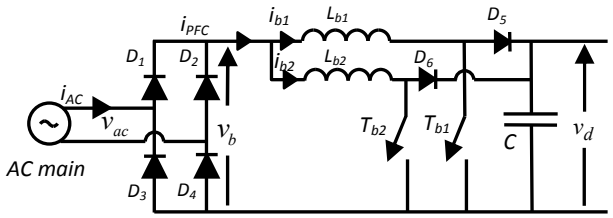
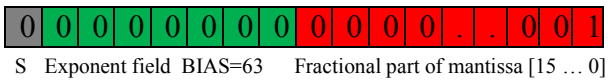


Fig. 2. Implemented dual boost PFC topology.

The switching losses reduction effect comes from the different values of both the switching frequency and current amplitude of each switch. In particular for the first switch (main switch) high currents and low switching frequency are used, while for the second switch (filtering switch) the control algorithm imposes high switching frequency and low current.

Because the speed of a classical DSP is not suitable to implement the proposed quasi-analog current control a low cost FPGA has been used to control a 2 kW prototype converter.

The authors have developed a floating point math library for FPGAs, called *sfloat24* [5] [6] [7] [8], which is used, in this paper, for the implemented control strategies. Respects to the classical IEEE 754 floating point number format, numbers are represented by a 24 bit word length. This reduced representation is useful when a low cost FPGA device is used. Using this library the smallest number, neglecting the sign (Most Significant Bit), is represented by the following word:



S Exponent field BIAS=63 Fractional part of mantissa [15 … 0]

that corresponds to the decimal value of $1.08423e^{-19}$, the greatest value is represented by:

S Exponent field BIAS=63 Fractional part of mantissa [15 … 0]

that corresponds to: $1.84467e^{+19}$.

The implementation of the basic arithmetic operations and of the saturation operator allows to implement the PI controller and the Active Filtering control strategy.

The FPGA-based controllers offer the advantages such as high speed, possibility of inclusion in complex algorithms, and low power consumption.

III. MODELLING OF A DIGITAL PID CONTROLLER

A PID regulator consists of three basic modules, the Proportional module, the Integral and the Derivative module. In order to use this controller it is necessary to define the used modules (P, I or D) and specify the respective parameters [9] [10] [11].

The control actions are shown in the following Fig.:

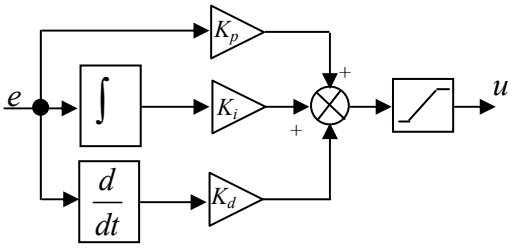


Fig. 3. Topology of a PID Controller

The mathematical expression of a generic PID controller is:

$$u(t) = K_p \cdot e(t) + K_i \cdot \int_0^t e(t) \cdot dt + K_d \cdot \frac{d}{dt} e(t) \qquad (1)$$

$$u(t) = Kp \cdot \left[e(t) + \frac{1}{T_i} \int_0^t e(t) \cdot d(t) + T_d \cdot \frac{d}{dt} e(t) \right] \qquad (2)$$

where K_p is the proportional gain, T_i is the integral time constant and T_d is the derivative time constant. In order to envisage a digital implementation, (2) must be formulated in a discrete time and for a small sampling time T_s, the difference equation is:

$$u(n) = K_p \cdot \left[e(n) + \frac{T_s}{T_i} \sum_{j=0}^{n} e(j) + \frac{T_d}{T_s} \cdot [e(n) - e(n-1)] \right] \qquad (3)$$

Usually, the derivative term in (3), can be neglected. Consequently the PI controller can be formulated as:

$$u(t) = K_p \cdot e(t) + K_i \cdot \int_0^t e(t) \cdot dt \qquad (4)$$

In this case the equation (3) can be rewritten as:

$$u(n) = K_p \cdot \left[e(n) + \frac{T_s}{T_i} \sum_{j=0}^{n} e(j) \right] \qquad (5)$$

IV. Dual Boost Converter, Modelling and Controlling

A dual boost converter, with reference to Fig. 2, can be described, considering all possible modes of working in Continuous Conduction Mode (CCM), by the following state space equations. The index k denotes the switching modes. The external input is assumed to be constant during every mode.
Therefore results:

$$\begin{aligned} \dot{x} &= A_k \cdot x + B \cdot u \\ y &= C \cdot x \end{aligned} \tag{6}$$

with:

$$k=1,..,4;\ \ k=1 \rightarrow f_{b1}=0, f_{b2}=0;\ k=2 \rightarrow f_{b1}=1, f_{b2}=1;$$
$$k=3 \rightarrow f_{b1}=1, f_{b2}=0;\ k=4 \rightarrow f_{b1}=0, f_{b2}=1;$$

The state variables are represented by $x = \begin{bmatrix} i_{b1} \\ i_{b2} \\ v_d \end{bmatrix}$ and u is the input voltage.

$$A_k(f_{b1}, f_{b2}) = \begin{bmatrix} -\frac{R_{b1}}{L_{b1}} & 0 & -\frac{1}{L_{b1}} \cdot (f_{b1}) \\ 0 & -\frac{R_{b2}}{L_{b2}} & -\frac{1}{L_{b2}} \cdot (f_{b2}) \\ \frac{1}{C} \cdot (f_{b1}) & \frac{1}{C} \cdot (f_{b2}) & -\frac{1}{R \cdot C} \end{bmatrix}$$

$$B = \begin{bmatrix} \frac{1}{L_{b1}} \\ \frac{1}{L_{b2}} \\ 0 \end{bmatrix} \qquad C = \begin{bmatrix} 1 & 0 & 0 \\ 0 & 1 & 0 \\ 0 & 0 & 0 \end{bmatrix}$$

The matrix A_k is depending by the power switches state, while the matrices B and C don't vary if the converter works in CCM. The above matrices are written by neglecting the stray parameters of the converter [12], in this case the output voltage of the boost converter is equal to the voltage across the capacitor C, as depicted in Fig. 2.

The full control of the PFC i_{b1} and i_{b2} currents can be achieved only if the conditions depicted in [13] are satisfied.
The following expressions represent main and filtering commutation functions.

$$f_{b1} = \begin{cases} 0 & \text{if } T_{b1}=1 \text{ (closed switch)} \\ 1 & \text{if } T_{b1}=0 \text{ (opened switch)} \end{cases} \tag{7}$$

$$f_{b2} = \begin{cases} 0 & \text{if } T_{b2}=1 \text{ (closed switch)} \\ 1 & \text{if } T_{b2}=0 \text{ (opened switch)} \end{cases} \tag{8}$$

By means (7) and (8) the control of the PFC currents i_{b1} and i_{b2} can be achieved and, in particular, it is possible to track the desired value of both the PFC reference currents evaluated by using the control scheme of Fig. 1.
The main goal of the implemented dual boost PFC and of the above described control algorithm is to introduce improvements in terms of power losses reduction [14] thanks to the Active Filtering (AF) approach.

V. Simulation Results

To validate the depicted Dual Boost PFC control strategy, using the developed *sfloat24* math library, several simulations have been performed.
The simulations have been performed using the Altera® DSP Builder 9.1 tool under Matlab®.
It is important to underline that the use of the Altera® DSP Builder allows to preliminary simulate the algorithm and then to program directly the FPGA starting from the Simulink® code.
The HDL import block has been used to import in Simulink® the used *sfloat24* math operators.
In all the tests results that the implemented *sfloat24* math operators have a latency time at maximum of 6 clock cycles.

In Fig. 4a the main PFC current obtained with a hysteresis band of 5 A is shown; while in Fig. 4b the filtering PFC current obtained with a hysteresis band of 1 A is depicted.

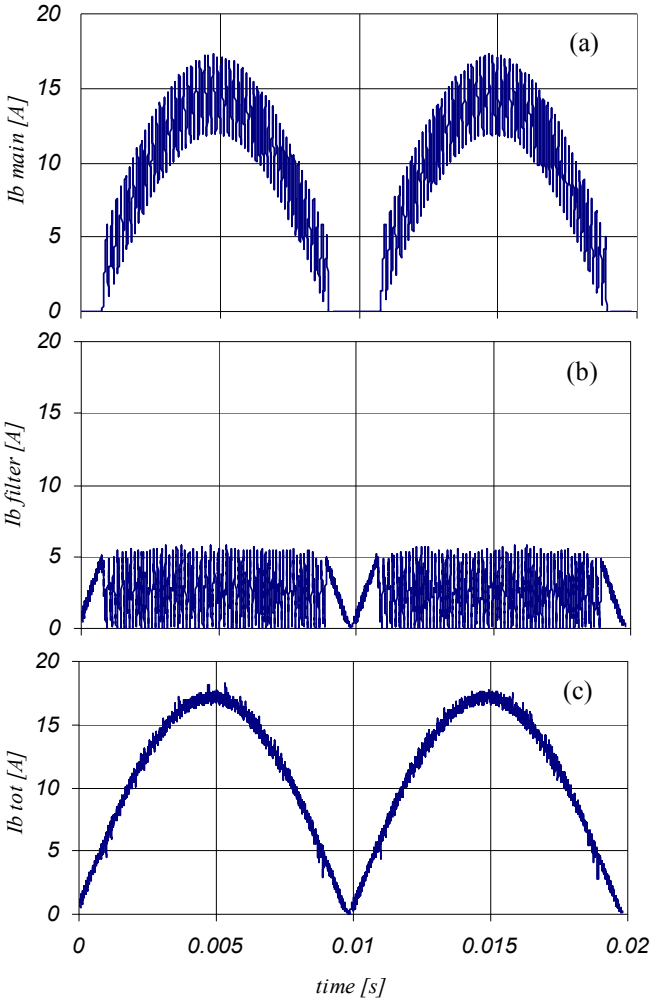


Fig. 4. Simulation results: Main PFC current (a), Filtering PFC current (b) and (c) total boost current (c).

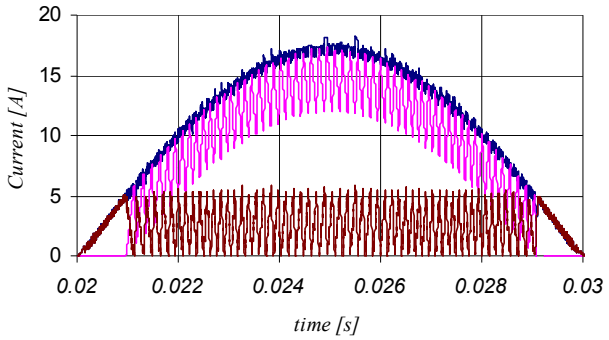


Fig. 5. Simulation results: Active filtering principle.

Fig. 5 highlights the Active Filtering principle. The global PFC current (blue colour) represents the output of the PI regulator multiplied by a modulo sine, obtained as explained in the next section.

VI. EXPERIMENTAL RESULTS

After the simulations several experiments have been done, the experimental setup has been implemented on an ALTERA® EP1C6Q240C6 low cost FPGA device and using, as power converter, a 2 kW dual boost PFC based on SK 60 GAL 123 SEMIKRON® power devices. The main and filtering chokes are respectively L_{b1}=2.71 mH and L_{b2}=1.2 mH, the capacitance C, see Fig. 1, is 1100 µF, this system feeds a DC load of 100 Ω.

The PI parameters are: K_p=0.8, K_i=0.008 and the reference current is limited to 20A. The output reference voltage, in all the simulations and experimental tests has been fixed to 450V.

In the implemented control strategy the sensed currents are the main PFC current, the filtering PFC current and optionally, only in order to validate the tests, the AC line current is sensed. To perform the experimental tests is strictly necessary to acquire the AC line voltage or the boost voltage in order to generate a *modulo sine,* function needed for "building" the reference current at input of the adopted feeding algorithm. To keep the output voltage to a desired value is also necessary to acquire also the output DC voltage.

In order to sense the currents the LEM® LA25 NP Hall effect current transducers have been used and to sense the voltages the LEM® LV25 P Hall effect voltage transducers have been used. A block diagram of the experimental setup is depicted in Fig. 6. The reference current is generated by scaling the absolute value of the AC line voltage multiplying by a factor, less than unity, in order to obtain the desired current reference.

Unfortunately the Cyclone® I EP1C6Q240C6 evaluation board has not provided of an analog to digital (A/D) unit section. To acquire the analog signals proportional to sensed voltages, main and filtering PFC currents, an analog to digital board based on 10 bit National Semiconductor® AD1061CN A/D converters has been built up and connected to used FPGA device.

The chosen A/D converter, by the evaluation of the quantizer error and by its high speed, is widely suited for the proposed experimental layout.

This A/D converter executes a conversion in only 2 µS, the main task time execution of the control algorithm has been set to 2.5 µS.

The A/D quantization error, Q_e, has been evaluated by using the following well-known relation:

$$Q_e = \frac{V_{ref}}{2^{conversion\_bits}} = \frac{5}{1024} = 0.0049 \qquad (9)$$

where V_{ref} is the A/D reference voltage.

The handshaking of the A/D converters with the used FPGA device has been implemented writing the following code, it has been written taking in count the technical specifications, depicted in the datasheet.

```
ad_process : process (aux_adwr_net, ad_main_int_net)
  begin
   if(aux_adwr_net<='0' and ad_main_int_net<='0') then
      ad_main_rd_net<=aux_adwr_net;
      ad_main_value_net<=ad_main_input_net after 50ns;
   end if;
end process ad_process;
```

This fragment code, for example, manages a single A/D converter, for the management of a multiple A/D conversion the code is quite similar.

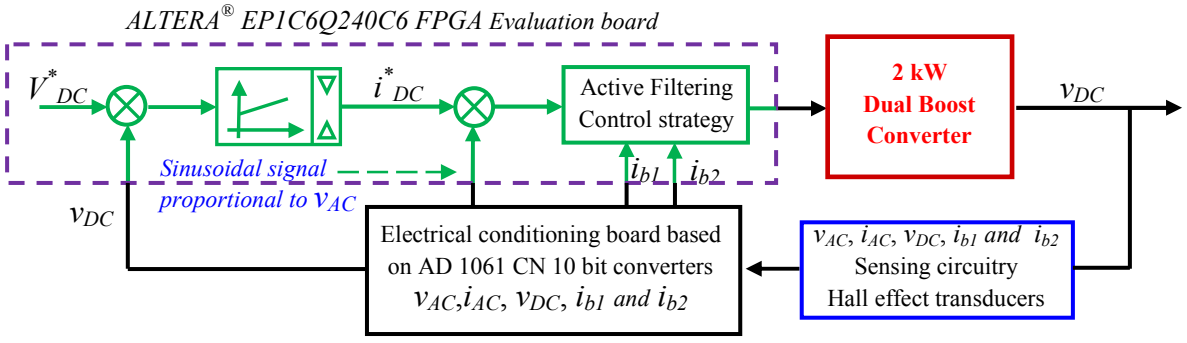


Fig. 6. Block diagram of implemented control strategy

In the Table I is depicted the total logic elements used by the implemented control strategy in the case of single PFC configuration and when the Active Filtering approach is used.

TABLE I
IMPLEMENTED CONTROL STRATEGY, FPGA DEVICE OCCUPATION

Implemented Control strategy: A/D handshaking, PI Controller and AF control strategy.	Total logic elements
Single PFC: Classical configuration	3545/5980 [59%]
Double PFC: Active Filtering configuration	5213/5980 [87%]

The following Fig. shows, in conceptual manner, the implemented *sfloat24* digital PI controller.

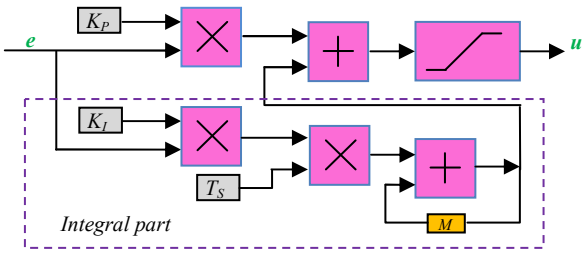


Fig. 7. Graphical description of the *PI* algorithm. The magenta coloured blocks are the *sfloat24* math elements. A memory block (yellow coloured) is necessary to execute in correct manner the integration operation.

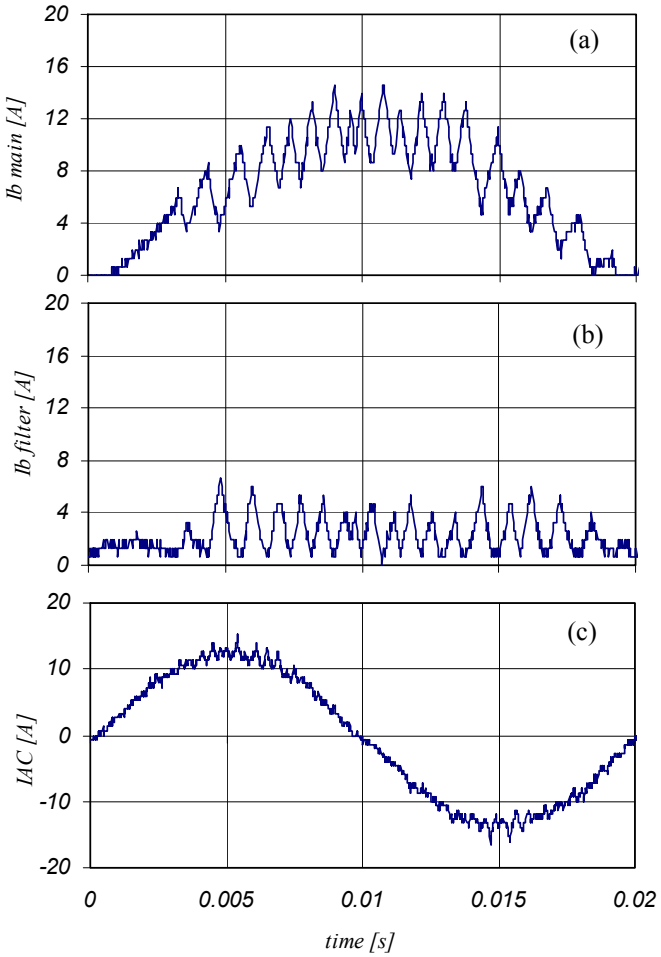


Fig. 8. Experimental results: Main PFC current (a), Filtering current (b) and AC main current (c).

In Fig. 8 the currents waveforms obtained with the dual boost converter are shown. The main converter works with a switching frequency of 6 kHz and a current of 15 A. The filtering converter instead works with a current of 5 A and a switching frequency of 37 kHz.
In Fig. 9 is shown a detail of both the *main PFC* current and the *filtering PFC* current in order to highlight the active filtering principle. In Fig. 10, instead, are shown the results obtained by working, with the same prototype board, in the single PFC operating mode. In this case, to obtain the same current quality, the converter works with a current of 15 A at switching frequency of 20 kHz.

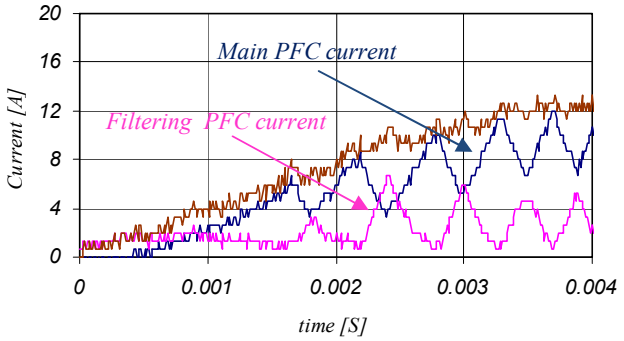


Fig. 9. Experimental results – Detail of main PFC current and filtering PFC current.

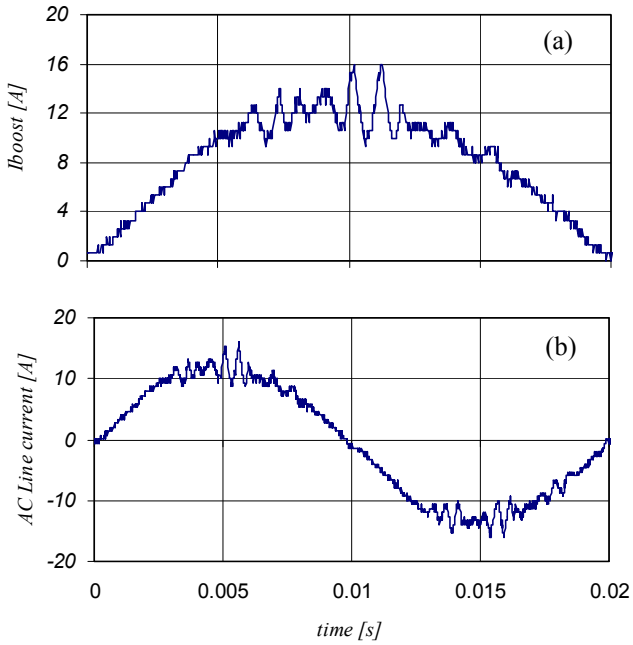


Fig. 10. Experimental results: Boost current (a) and AC main current (b), in the case of single PFC operating mode.

To evaluate the efficiency improvements obtained by using the proposed approach several thermal tests have been performed.
In particular in Fig. 11 a thermal image of the tested circuit working in single boost mode (the *filtering PFC* is disabled) is shown.

As it is possible to see the heat sink temperature, close to the power device, reaches 58 °C while, in dual boost mode, working at the same operating condition (current ripple, reference current amplitude and DC bus voltage), is 47 °C, as shown in Fig. 12.

This means that a total losses reduction of 36% (*main* and *filtering* switching and conduction losses) has been obtained; these results confirm the validity of the implemented PFC scheme.

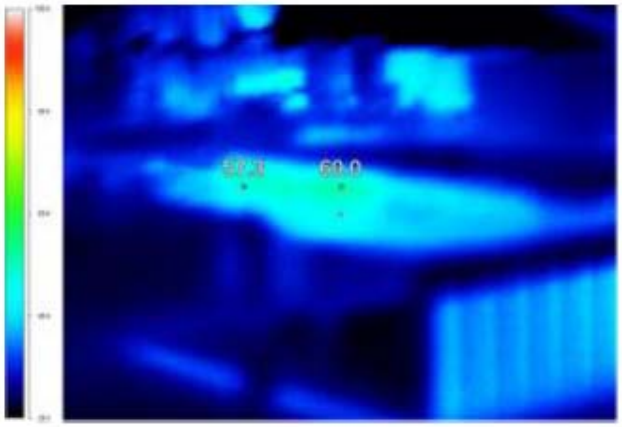


Fig. 11: Experimental results – thermal image of the tested circuit working in single mode.

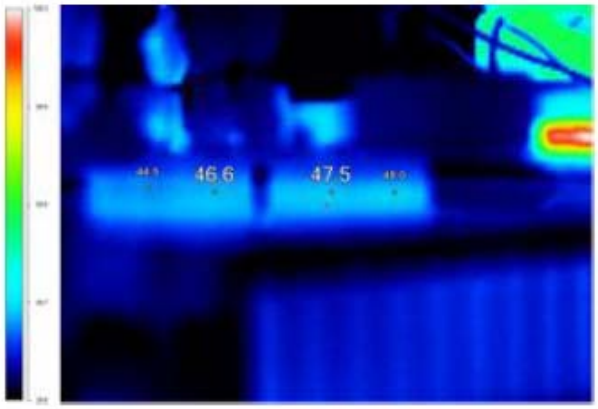


Fig. 12. Experimental results – thermal image of the tested circuit working in dual mode.

VII. CONCLUSIONS

A full (PI and power Active Filtering principle) current hysteresis controller, implemented in FPGA technology, is a configurable controller in terms of latency, resolution, and parallelism. The speed execution or latency of the implemented controller can be precisely controlled with the amount of reuse of *sfloat24* arithmetic elements.

Furthermore the developed *sfloat24* math library has been tested giving excellent results.

The implemented control for Parallel Power Factor Correction (PFC) scheme is based on an optimized power sharing where the active filtering approach is used to increase the current quality, and at the same time, to reduce the switching losses. In particular the experimental results show that the proposed approach achieves near unity power factor and a not negligible switching losses reduction.

REFERENCES

[1] Yuen Fong Chan, M. Moallem, and Wei Wang "Design and Implementation of Modular FPGA-Based PID Controllers" IEEE Transactions on Industrial Electronics, Vol. 54, N. 4, August 2007, pp. 1898-1906.

[2] Jappe, T.K.; Mussa, S.A.; Rosendo, R.H.S" Synchronous state machine inner FPGA controlling PFC boost converter", IEEE International Symposium on Industrial Electronics (ISIE),4-7 July 2010,pp. 1097-1102.

[3] Sanchez, D.F.,Llanos, C.H. and Ayala-Rincon, M."FPGA Based floating-point library for CORDIC algorithms", Programmable Logic Conference (SPL),24-26 March 2010,pp. 55-60.

[4] Chung-Wen Hung,Tsun-Hsi Chang, Chen-Yo Lin and Jhih-Han Chen"A NIOS II Base Wide Output Range Power Factor Corrector",IEEE TENCON 2011,21-24 November 2011,pp.817 - 821.

[5] IEEE Standard for Binary Floating-Point Arithmetic. (1985). ANSI/IEEE 754 1985.

[6] Xiaoming Tang, Tao Zhang, Zhenjie Wang and Wenliang Yuan, "A Novel Data F onnat Conversion Method Based on FPGA"Cross Strait Quad-Regional Radio Science and Wireless Technology Conference (CSQRWC),26-30 July 2011,pp. 1204 - 1207.

[7] F. Parillo, M.C. Miglionico "A Current Hysteresis Controller for Reduction of Switching Losses in a Full-Bridge Inverter "FPGA implementation by using a custom developed 24 bit Floating Point Math Library", IEEE International Universities Power Engineering Conference, UPEC 2011, 5 - 8 September 2011, pp: 1 – 6, Print ISBN: 978-3-8007-3402-3.

[8] F. Parillo, M.C. Miglionico "MODELLING A NEURON USING A CUSTOM MATH LIBRARY sfloat24 – IMPLEMENTATION OF A SIGMOID FUNCTION ON A FPGA DEVICE –", ISHAP Conference Sorrento Italy: 15 - 18 June 2011, http://204.202.238.22/isahp2011/dati/autor.html, Online Proceedings ISSN 1556-8296, Proceedings of the International Symposium on the Analytic Hierarchy Process for Multicriteria Decision Making, Publication date: The 11th ISAHP June 15, 2011.

[9] V. Subasri , K. Lavanya and B. Umanmaheswari, "Implementation of Digital PID controller in Field Programmable Gate Array (FPGA)" Power Electronics, 2006. IICPE 2006. India International Conference, pp. 172 – 176.

[10] L. Samet, N. Masmoudi, M. W. Kharrat, and L. Kamoun, "A digital PID controller for real-time and multi-loop control: A comparative study," in Proc. IEEE Int. Conf. Electron., Circuits and Syst., Sep. 1998, vol. 1, pp. 291–296.

[11] F. Parillo, M.C. Miglionico "FPGA implementation of sfloat24 digital PI", IEEE Conference PEDES Power India date: 20 - 23 December 2010.

[12] P. Schutyser, P. Gupta, A. Patra, "Stability Analysis of a Switching Control Strategy for DC-DC Boost Converter" India Annual Conference 2004, 20–22.12.2004, pp. 187-190.

[13] C. Attaianese, V. Nardi, F. Parillo, G. Tomasso, "Dual Boost High performances Power Factor Correction (PFC)", Twenty third IEEE Applied Power Electronics Conference (APEC 2008), Austin (USA),24-28.02.2008, pp. 1027-1032.

[14] N. Mohan, T.M. Undeland, W.P. Robins. Power Electronics: Converters, Applications and Design. John Wiley & Son, 2003.